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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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1. Overview

The M16C/26 group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 48-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, office/communications/portable/industrial equipment, etc

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.1 lists performance outline of M16C/26 group.

Table 1.1. Performance outline of M16C/26 group

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		50 ns (f(BCLK)= 20MHz, V _{CC1} = 3.0V to 5.5V) 100 ns (f(BCLK)= 10MHz, V _{CC1} = 2.7V to 5.5V)
Memory capacity	ROM	(See the product list)
	RAM	(See the product list)
I/O port	P15 to P17, P6, P7, P80 to P83, P85 to P87, P90 to P93, P10	8bit x 3, 7bit x 1, 4bit x 1, 3bit x 1
Multifunction timer		Timer A: 16 bits x 5 channels (TA0, TA1, TA2, TA3, TA4) Timer B: 16 bits x 3 channels (TB0, TB1, TB2) Three-phase Motor Control Timer
Serial I/O		2 channels (UART0, UART1) UART, clock synchronous 1 channels (UART2) UART, clock synchronous, I ² C bus ¹ , or IEBus ²
A/D converter		10 bits x 8 channels
DMAC		2 channels (trigger: 20 sources)
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		20 internal and 7 external sources, 4 software sources, 7 levels
Clock generation circuit		3 circuits } (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator) • Main clock • Sub-clock • On-chip oscillator(main-clock oscillation stop detect function)
Power supply voltage		V _{CC} =3.0V to 5.5V (f(BCLK)=20MHz) V _{CC} =2.7V to 5.5V (f(BCLK)=10MHz)
Flash memory	Program/erase voltage	V _{CC} =2.7V to 5.5V
	Number of program/erase	100 times (all area) 1000times (program area) /10000 times ³ (data area)
Power consumption		16mA (V _{CC} =3V, f(BCLK)=20MHz) 25μA (f(BCLK)=f(XCIN)=32kHz on RAM) 1.8μA (V _{CC} =3V, f(XCIN)=32kHz, when wait mode) 0.7μA (V _{CC} =3V, when stop mode)
I/O characteristics	I/O withstand voltage	5.0V
	Output current	5mA
Operating ambient temperature		-20 to 85°C -40 to 85°C ³
Device configuration		CMOS high performance silicon gate
Package		48-pin plastic mold QFP

Notes:

1. I²C bus is a trademark of Koninklijke Philips Electronics N.V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See Table 1.3 for the number of program/erase and the operating ambient temperature.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/26 group.

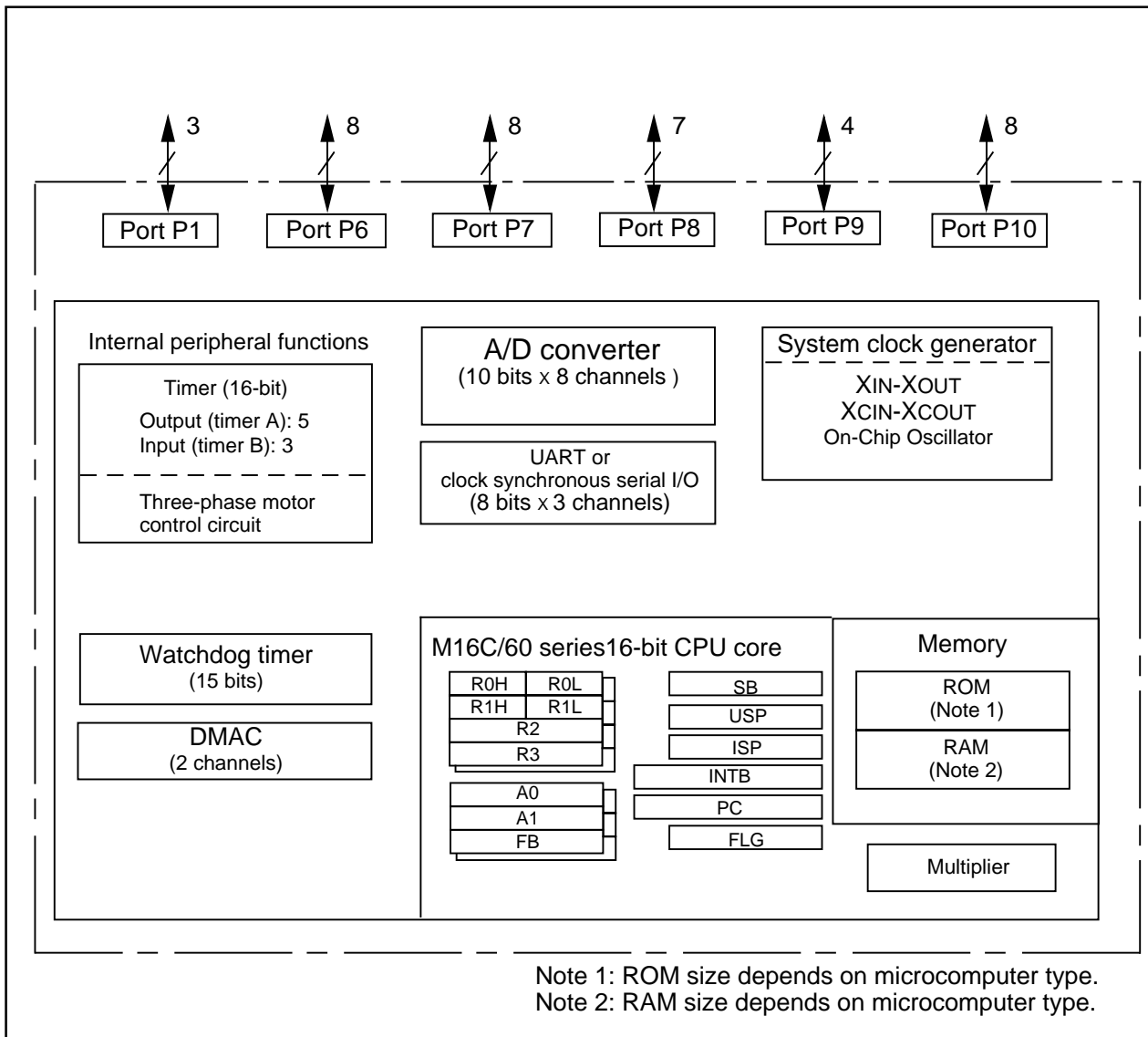


Figure 1.1. Block Diagram

1.4 Product List

Table 1.2 lists the M16C/26 group products, Figure 1.2 shows the type numbers, memory sizes and packages, Table 1.3 lists the product code, and Figure 1.3 shows the marking.

Table 1.2. Product List

As of May 2004

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30262F3GP	24K + 4K byte	1K byte	48P6Q-A	Flash ROM Version
M30262F4GP	32K + 4K byte	1K byte		
M30262F6GP	48K + 4K byte	2K byte		
M30262F8GP	64K + 4K byte	2K byte		

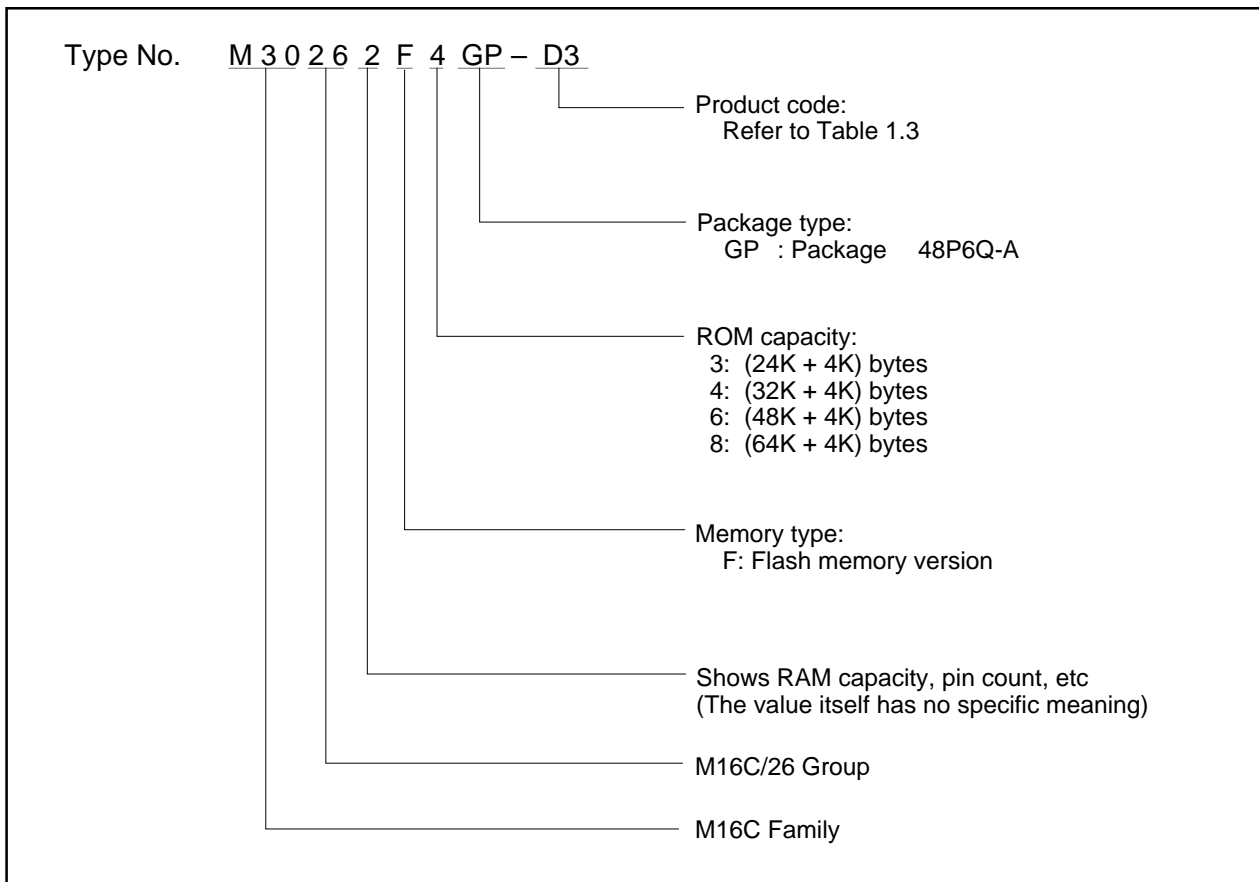
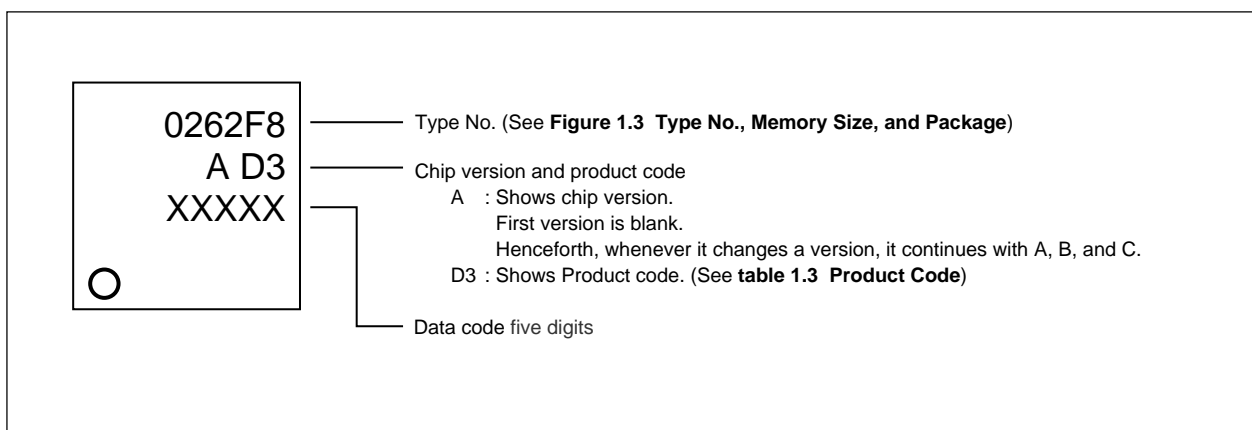


Figure 1.2. Type No., Memory Size, and Package

Table 1.3. Product code

Product Code	Package	Internal ROM (Program area)		Internal ROM (Data area)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
D3	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
D5					-20°C to 85°C	
D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
D9				-20°C to 85°C	-20°C to 85°C	
U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
U5					-20°C to 85°C	
U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
U9					-20°C to 85°C	-20°C to 85°C

**Figure 1.3. Marking Diagram of Flash Memory version for M16C/26 (Top View)**

1.5 Pin Configuration

Figures 1.4 showd the pin configurations (top view).

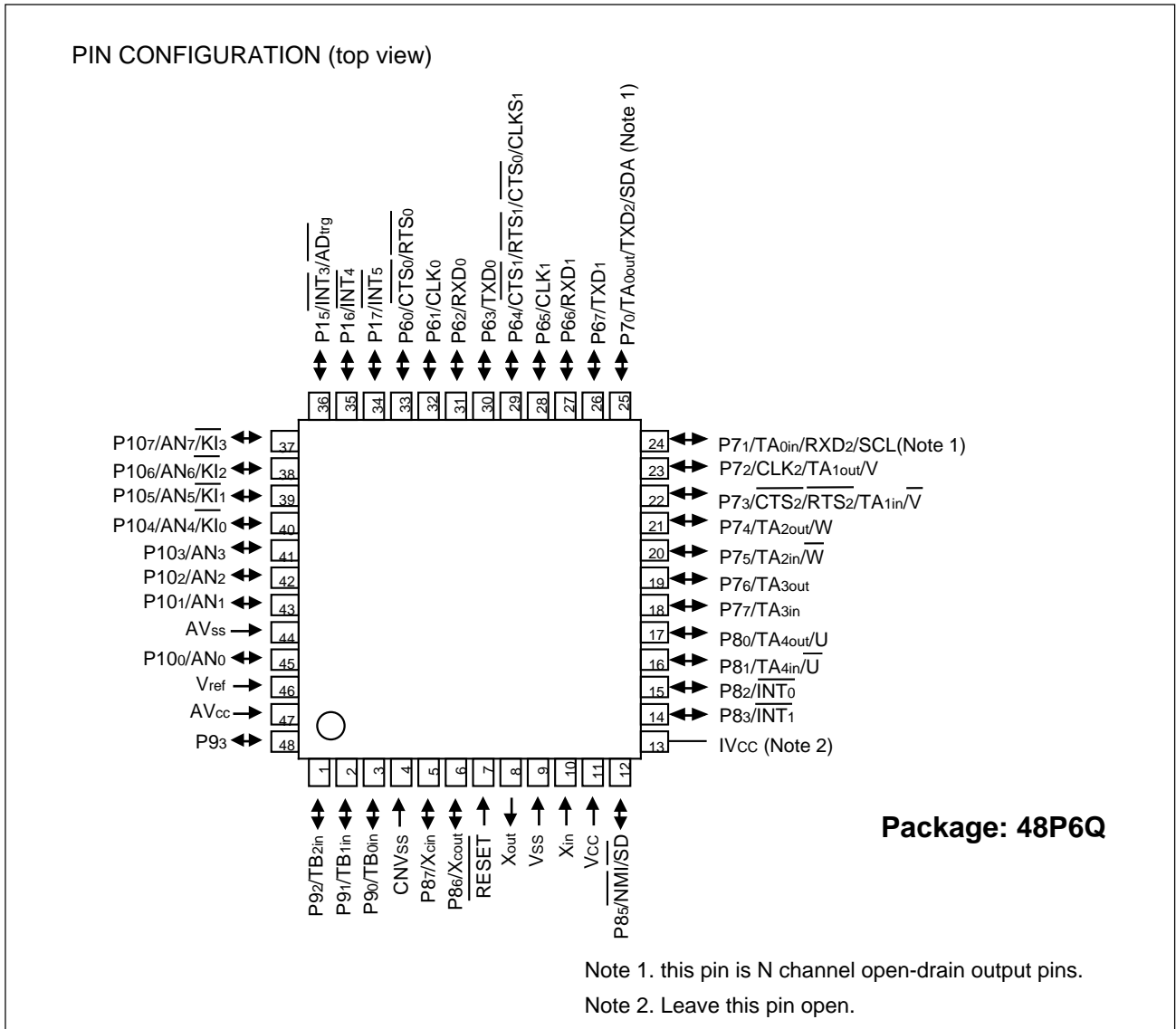


Figure 1.4. Pin Configuration (Top View)

1.6 Pin Description

Table 1.4 and 1.5 describe the available pins.

Table 1.4. Pin Description(1)

Pin name	Signal name	I/O type	Function
V _{CC} , V _{SS}	Power supply input		Apply 2.7V to 5.5V to the V _{CC} pin, and 0V to the V _{SS} pin.
CNV _{SS}	CNV _{SS}	Input	Connect this pin to V _{SS} .
IV _{CC}	IV _{CC}		Leave this pin open.
RESET	Reset input	Input	"L" on this input resets the microcomputer.
X _{IN} X _{OUT}	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or crystal between the X _{IN} and the X _{OUT} pins. To use an externally derived clock, input it to the X _{IN} pin and leave the X _{OUT} pin open.
AV _{CC}	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to V _{CC} .
AV _{SS}	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to V _{SS} .
V _{REF}	Reference Voltage input	Input	This pin is a reference voltage input for the A/D converter.
P ₁₅ ~P ₁₇	I/O port P1	Input/ output	This is an 3-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resistor option can be selected for the entire group of three pins. Additional software selectable secondary functions are: 1) P ₁₅ to P ₁₇ can be configured as external $\overline{\text{INT}}$ interrupt pins, and; 2) P ₁₅ can input a trigger for the A/D converter.
P ₆₀ ~P ₆₇	I/O port P6	Input/ output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resistor option can be selected for the entire group of four pins. Pins in this port also function as UART0 and UART1 I/O.
P ₇₀ ~P ₇₇	I/O port P7	Input/ output	This is an 8-bit I/O port equivalent to P6. (P ₇₀ and P ₇₁ are N channel open-drain output) P7 can also function as I/O for timer A0 to A3, as selected by software. Additional programming options are: P ₇₀ to P ₇₃ can assume UART2 I/O capabilities, and P ₇₂ to P ₇₅ can function as output pins for the three-phase motor control timer.
P ₈₀ ~P ₈₃ , P ₈₅ ~P ₈₇	I/O port P8	Input/ output	P ₈₀ to P ₈₃ and P ₈₅ to P ₈₇ are an 7-bit I/O port equivalent to P6. When used for input, a pull-up resistor option can be selected for the entire group of four pins or three pins. Additional software-selectable secondary functions are: 1) P ₈₀ and P ₈₁ can act as either I/O for Timer A4, or as output pins for the three-phase motor control timer; 2) P ₈₂ to P ₈₃ can be configured as external $\overline{\text{INT}}$ interrupt pins; 3) P ₈₅ can be used as $\overline{\text{NMI/SD}}$. P ₈₅ can not be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to P ₈₅ after setting the direction register for P ₈₅ to "0" when the three-phase motor control is enabled, and; 4) P ₈₆ and P ₈₇ can serve as I/O pins for the sub-clock generation circuit. In this latter case, a quartz oscillator must be connected between P ₈₆ (X _{COU} T pin) and P ₈₇ (X _{CIN} pin).

Table 1.7. Pin Description(2)

Pin name	Signal name	I/O type	Function
P9 ₀ ~P9 ₃	I/O port P9	Input/ output	This is an 4-bit I/O port equivalent to P6. Additional software-selectable secondary functions are: 1) P9 ₀ to P9 ₂ can act as Timer B0~B2 input pins.
P10 ₀ ~P10 ₇	I/O port P10	Input/ output	This is an 8-bit I/O port equivalent to P6. This port can also function as A/D converter input pins, as selected by software. Furthermore, P10 ₄ to P10 ₇ can also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

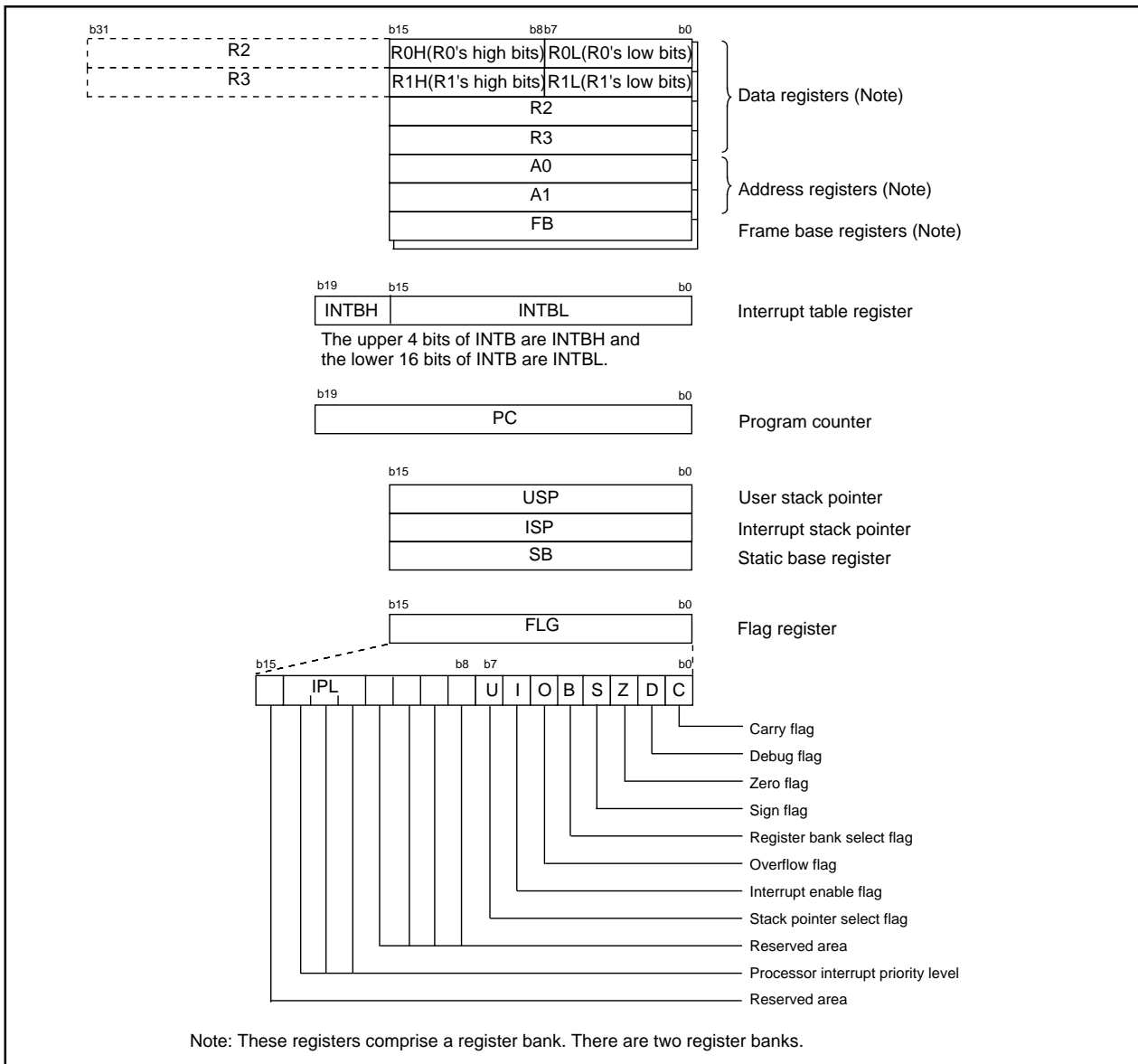


Figure 2.1. Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/26 group. The address space extends the 1M bytes from address 00000₁₆ to FFFFF₁₆.

The internal ROM is allocated in a lower address direction beginning with address FFFFF₁₆. For example, a 32-Kbyte internal ROM is allocated to the addresses from F8000₁₆ to FFFFF₁₆.

The fixed interrupt vector table is allocated to the addresses from FFFDC₁₆ to FFFFF₁₆. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400₁₆. For example, a 1-Kbytes internal RAM is allocated to the addresses from 00400₁₆ to 007FF₁₆. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SRF is allocated to the addresses from 00000₁₆ to 003FF₁₆. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00₁₆ to FFFDB₁₆. This vector is used by the JMPS or JSRS instruction. For details, refer to the “M16C/60 and M16C/20 Series Software Manual.”

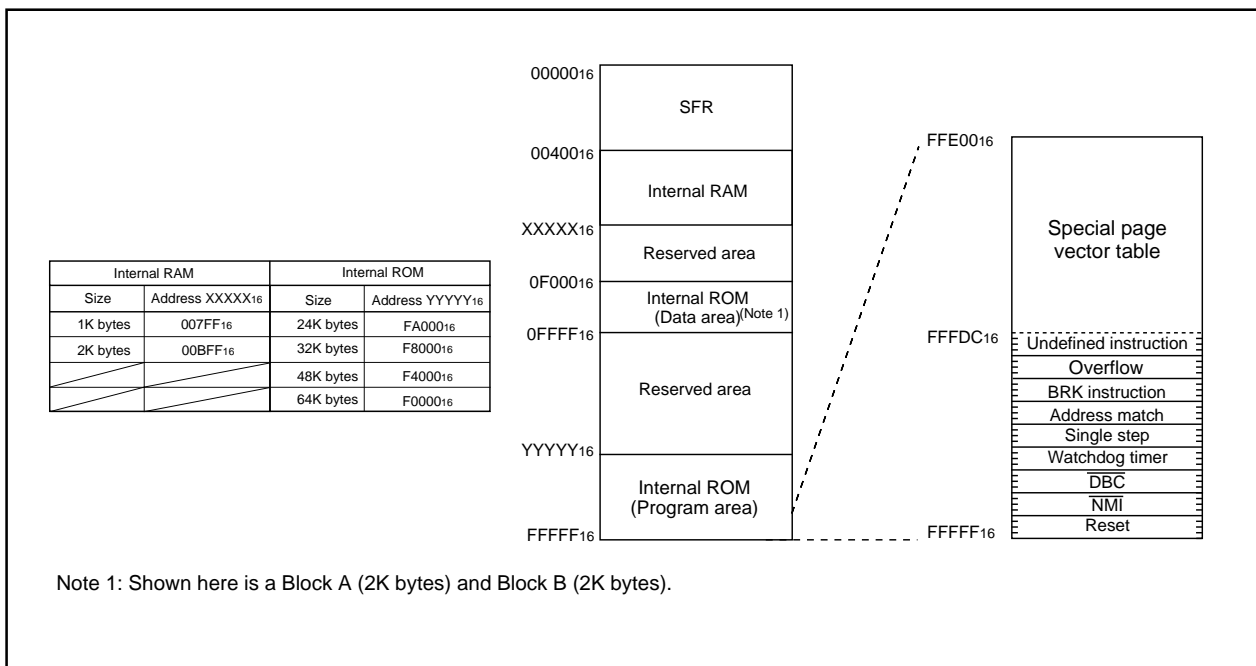


Figure 3.1. Memory Map

4. Special Function Register (SFR) Map

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0 (Note 2)	PM0	00 ₁₆
0005 ₁₆	Processor mode register 1	PM1	00001000 ₂
0006 ₁₆	System clock control register 0	CM0	01001000 ₂
0007 ₁₆	System clock control register 1	CM1	00100000 ₂
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX00 ₂
000A ₁₆	Protect register	PRCR	XX000000 ₂
000B ₁₆			
000C ₁₆	Oscillation stop detection register (Note 3)	CM2	0X000000 ₂
000D ₁₆			
000E ₁₆	Watchdog timer start register	WDTS	XX ₁₆
000F ₁₆	Watchdog timer control register	WDC	00XXXXXX ₂ (Note 4)
0010 ₁₆	Address match interrupt register 0	RMAD0	00 ₁₆
0011 ₁₆			00 ₁₆
0012 ₁₆			X0 ₁₆
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	00 ₁₆
0015 ₁₆			00 ₁₆
0016 ₁₆			X0 ₁₆
0017 ₁₆			
0018 ₁₆			
0019 ₁₆	Voltage detection register 1 (Note 5)	VCR1	00001000 ₂
001A ₁₆	Voltage detection register 2 (Note 5)	VCR2	00 ₁₆
001B ₁₆			
001C ₁₆			
001D ₁₆			
001E ₁₆	Processor mode register 2	PM2	XXX00000 ₂
001F ₁₆	Voltage down detection interrupt register	D4INT	00 ₁₆
0020 ₁₆	DMA0 source pointer	SAR0	XX ₁₆
0021 ₁₆			XX ₁₆
0022 ₁₆			XX ₁₆
0023 ₁₆			
0024 ₁₆	DMA0 destination pointer	DAR0	XX ₁₆
0025 ₁₆			XX ₁₆
0026 ₁₆			XX ₁₆
0027 ₁₆			
0028 ₁₆	DMA0 transfer counter	TCR0	XX ₁₆
0029 ₁₆			XX ₁₆
002A ₁₆			
002B ₁₆			
002C ₁₆	DMA0 control register	DM0CON	00000X00 ₂
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆	DMA1 source pointer	SAR1	XX ₁₆
0031 ₁₆			XX ₁₆
0032 ₁₆			XX ₁₆
0033 ₁₆			
0034 ₁₆	DMA1 destination pointer	DAR1	XX ₁₆
0035 ₁₆			XX ₁₆
0036 ₁₆			XX ₁₆
0037 ₁₆			
0038 ₁₆	DMA1 transfer counter	TCR1	XX ₁₆
0039 ₁₆			XX ₁₆
003A ₁₆			
003B ₁₆			
003C ₁₆	DMA1 control register	DM1CON	00000X00 ₂
003D ₁₆			
003E ₁₆			
003F ₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.

Note 2: The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.

Note 3: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.

Note 4: The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program. It is set to "0" when the input voltage at the V_{CC1} pin drops to V_{dct2} or less while the VC25 bit in the VCR2 register is set to "1" (RAM retention limit detection circuit enable).

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆	INT3 interrupt control register	INT3IC	XX00X0002
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆	INT5 interrupt control register	INT5IC	XX00X0002
0049 ₁₆	INT4 interrupt control register	INT4IC	XX00X0002
004A ₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX0002
004B ₁₆	DMA0 interrupt control register	DM0IC	XXXXX0002
004C ₁₆	DMA1 interrupt control register	DM1IC	XXXXX0002
004D ₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E ₁₆	A/D conversion interrupt control register	ADIC	XXXXX0002
004F ₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX0002
0050 ₁₆	UART2 receive interrupt control register	S2RIC	XXXXX0002
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 ₁₆	Timer A0 interrupt control register	TA0IC	XXXXX0002
0056 ₁₆	Timer A1 interrupt control register	TA1IC	XXXXX0002
0057 ₁₆	Timer A2 interrupt control register	TA2IC	XXXXX0002
0058 ₁₆	Timer A3 interrupt control register	TA3IC	XXXXX0002
0059 ₁₆	Timer A4 interrupt control register	TA4IC	XXXXX0002
005A ₁₆	Timer B0 interrupt control register	TB0IC	XXXXX0002
005B ₁₆	Timer B1 interrupt control register	TB1IC	XXXXX0002
005C ₁₆	Timer B2 interrupt control register	TB2IC	XXXXX0002
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E ₁₆	INT1 interrupt control register	INT1IC	XX00X0002
005F ₁₆			
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

Note :The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0080 ₁₆			
0081 ₁₆			
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
~			~
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆	Flash memory control register 4 (Note 2)	FMR4	01000002
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1 (Note 2)	FMR1	0100XX0X2
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0 (Note 2)	FMR0	XX0000012
01B8 ₁₆			
01B9 ₁₆			
01BA ₁₆			
01BB ₁₆			
01BC ₁₆			
01BD ₁₆			
01BE ₁₆			
01BF ₁₆			
~			~
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆			
025D ₁₆			
025E ₁₆	Peripheral clock select register	PCLKR	000000112
025F ₁₆			
~			~
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆			
0335 ₁₆			
0336 ₁₆			
0337 ₁₆			
0338 ₁₆			
0339 ₁₆			
033A ₁₆			
033B ₁₆			
033C ₁₆			
033D ₁₆			
033E ₁₆			
033F ₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.

Note 2: This register is included in the flash memory version.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0340 ₁₆			
0341 ₁₆			
0342 ₁₆	Timer A1-1 register	TA11	XX16
0343 ₁₆			XX16
0344 ₁₆	Timer A2-1 register	TA21	XX16
0345 ₁₆			XX16
0346 ₁₆	Timer A4-1 register	TA41	XX16
0347 ₁₆			XX16
0348 ₁₆	Three-phase PWM control register 0	INVC0	0016
0349 ₁₆	Three-phase PWM control register 1	INVC1	0016
034A ₁₆	Three-phase output buffer register 0	IDB0	0016
034B ₁₆	Three-phase output buffer register 1	IDB1	0016
034C ₁₆	Dead time timer	DTT	XX16
034D ₁₆	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX16
034E ₁₆			
034F ₁₆			
0350 ₁₆			
0351 ₁₆			
0352 ₁₆			
0353 ₁₆			
0354 ₁₆			
0355 ₁₆			
0356 ₁₆			
0357 ₁₆			
0358 ₁₆			
0359 ₁₆			
035A ₁₆			
035B ₁₆			
035C ₁₆			
035D ₁₆			
035E ₁₆			
035F ₁₆	Interrupt cause select register	IFSR	0016
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆			
0365 ₁₆			
0366 ₁₆			
0367 ₁₆			
0368 ₁₆			
0369 ₁₆			
036A ₁₆			
036B ₁₆			
036C ₁₆			
036D ₁₆			
036E ₁₆			
036F ₁₆			
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆	UART2 special mode register 4	U2SMR4	0016
0375 ₁₆	UART2 special mode register 3	U2SMR3	000X0X0X2
0376 ₁₆	UART2 special mode register 2	U2SMR2	X00000002
0377 ₁₆	UART2 special mode register	U2SMR	X00000002
0378 ₁₆	UART2 transmit/receive mode register	U2MR	0016
0379 ₁₆	UART2 bit rate generator	U2BRG	XX16
037A ₁₆	UART2 transmit buffer register	U2TB	XXXXXXXX2
037B ₁₆			XXXXXXXX2
037C ₁₆	UART2 transmit/receive control register 0	U2C0	000010002
037D ₁₆	UART2 transmit/receive control register 1	U2C1	000000102
037E ₁₆	UART2 receive buffer register	U2RB	XXXXXXXX2
037F ₁₆			XXXXXXXX2

Note : The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0380 ₁₆	Count start flag	TABSR	00 ₁₆
0381 ₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX ₂
0382 ₁₆	One-shot start flag	ONSF	00 ₁₆
0383 ₁₆	Trigger select register	TRGSR	00 ₁₆
0384 ₁₆	Up-down flag	UDF	00 ₁₆
0385 ₁₆			
0386 ₁₆ 0387 ₁₆	Timer A0 register	TA0	XX ₁₆ XX ₁₆
0388 ₁₆ 0389 ₁₆	Timer A1 register	TA1	XX ₁₆ XX ₁₆
038A ₁₆ 038B ₁₆	Timer A2 register	TA2	XX ₁₆ XX ₁₆
038C ₁₆ 038D ₁₆	Timer A3 register	TA3	XX ₁₆ XX ₁₆
038E ₁₆ 038F ₁₆	Timer A4 register	TA4	XX ₁₆ XX ₁₆
0390 ₁₆ 0391 ₁₆	Timer B0 register	TB0	XX ₁₆ XX ₁₆
0392 ₁₆ 0393 ₁₆	Timer B1 register	TB1	XX ₁₆ XX ₁₆
0394 ₁₆ 0395 ₁₆	Timer B2 register	TB2	XX ₁₆ XX ₁₆
0396 ₁₆	Timer A0 mode register	TA0MR	00 ₁₆
0397 ₁₆	Timer A1 mode register	TA1MR	00 ₁₆
0398 ₁₆	Timer A2 mode register	TA2MR	00 ₁₆
0399 ₁₆	Timer A3 mode register	TA3MR	00 ₁₆
039A ₁₆	Timer A4 mode register	TA4MR	00 ₁₆
039B ₁₆	Timer B0 mode register	TB0MR	00XX0000 ₂
039C ₁₆	Timer B1 mode register	TB1MR	00XX0000 ₂
039D ₁₆	Timer B2 mode register	TB2MR	00XX0000 ₂
039E ₁₆ 039F ₁₆	Timer B2 special mode register	TB2SC	XXXXXX00 ₂
03A0 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
03A1 ₁₆	UART0 bit rate generator	U0BRG	XX ₁₆
03A2 ₁₆ 03A3 ₁₆	UART0 transmit buffer register	U0TB	XXXXXXXX ₂ XXXXXXXX ₂
03A4 ₁₆	UART0 transmit/receive control register 0	U0C0	00001000 ₂
03A5 ₁₆	UART0 transmit/receive control register 1	U0C1	00000010 ₂
03A6 ₁₆ 03A7 ₁₆	UART0 receive buffer register	U0RB	XXXXXXXX ₂ XXXXXXXX ₂
03A8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
03A9 ₁₆	UART1 bit rate generator	U1BRG	XX ₁₆
03AA ₁₆ 03AB ₁₆	UART1 transmit buffer register	U1TB	XXXXXXXX ₂ XXXXXXXX ₂
03AC ₁₆	UART1 transmit/receive control register 0	U1C0	00001000 ₂
03AD ₁₆	UART1 transmit/receive control register 1	U1C1	00000010 ₂
03AE ₁₆ 03AF ₁₆	UART1 receive buffer register	U1RB	XXXXXXXX ₂ XXXXXXXX ₂
03B0 ₁₆ 03B1 ₁₆ 03B2 ₁₆ 03B3 ₁₆ 03B4 ₁₆ 03B5 ₁₆ 03B6 ₁₆ 03B7 ₁₆	UART transmit/receive control register 2	UCON	X0000000 ₂
03B8 ₁₆ 03B9 ₁₆	DMA0 request cause select register	DM0SL	00 ₁₆
03BA ₁₆ 03BB ₁₆ 03BC ₁₆ 03BD ₁₆ 03BE ₁₆ 03BF ₁₆	DMA1 request cause select register	DM1SL	00 ₁₆

Note : The blank areas are reserved and cannot be accessed by users.
X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
03C0 ₁₆ 03C1 ₁₆	A/D register 0	AD0	XXXXXXXX2 XXXXXXXX2
03C2 ₁₆ 03C3 ₁₆	A/D register 1	AD1	XXXXXXXX2 XXXXXXXX2
03C4 ₁₆ 03C5 ₁₆	A/D register 2	AD2	XXXXXXXX2 XXXXXXXX2
03C6 ₁₆ 03C7 ₁₆	A/D register 3	AD3	XXXXXXXX2 XXXXXXXX2
03C8 ₁₆ 03C9 ₁₆	A/D register 4	AD4	XXXXXXXX2 XXXXXXXX2
03CA ₁₆ 03CB ₁₆	A/D register 5	AD5	XXXXXXXX2 XXXXXXXX2
03CC ₁₆ 03CD ₁₆	A/D register 6	AD6	XXXXXXXX2 XXXXXXXX2
03CE ₁₆ 03CF ₁₆	A/D register 7	AD7	XXXXXXXX2 XXXXXXXX2
03D0 ₁₆			
03D1 ₁₆			
03D2 ₁₆			
03D3 ₁₆			
03D4 ₁₆ 03D5 ₁₆	A/D control register 2	ADCON2	0016
03D6 ₁₆	A/D control register 0	ADCON0	0000XXX2
03D7 ₁₆ 03D8 ₁₆	A/D control register 1	ADCON1	0016
03D9 ₁₆			
03DA ₁₆			
03DB ₁₆			
03DC ₁₆			
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆			
03E1 ₁₆ 03E2 ₁₆	Port P1 register	P1	XX16
03E3 ₁₆ 03E4 ₁₆	Port P1 direction register	PD1	0016
03E5 ₁₆			
03E6 ₁₆			
03E7 ₁₆			
03E8 ₁₆			
03E9 ₁₆			
03EA ₁₆			
03EB ₁₆			
03EC ₁₆	Port P6 register	P6	XX16
03ED ₁₆	Port P7 register	P7	XX16
03EE ₁₆	Port P6 direction register	PD6	0016
03EF ₁₆	Port P7 direction register	PD7	0016
03F0 ₁₆	Port P8 register	P8	XX16
03F1 ₁₆	Port P9 register	P9	XX16
03F2 ₁₆	Port P8 direction register	PD8	00X000002
03F3 ₁₆	Port P9 direction register	PD9	0016
03F4 ₁₆ 03F5 ₁₆	Port P10 register	P10	XX16
03F6 ₁₆	Port P10 direction register	PD10	0016
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆	Pull-up control register 0	PUR0	0016
03FD ₁₆	Pull-up control register 1	PUR1	0016
03FE ₁₆	Pull-up control register 2	PUR2	0016
03FF ₁₆	Port control register	PCR	0016

Note 1: The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 16.1. Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated value	Unit
V _{CC}	Supply voltage		V _{CC} =AV _{CC}	-0.3 to 6.5	V
AV _{CC}	Analog supply voltage		V _{CC} =AV _{CC}	-0.3 to 6.5	V
V _I	Input voltage	RESET, CNV _{SS} , P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, VREF, X _{IN}		-0.3 to V _{CC} +0.3	V
		P70, P71		-0.3 to 6.5	V
V _O	Output voltage	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, X _{OUT}		-0.3 to V _{CC} +0.3	V
		P70, P71		-0.3 to 6.5	V
P _d	Power dissipation		T _{opr} =25 °C	300	mW
T _{opr}	Operating ambient temperature			-20 to 85 / -40 to 85	°C
T _{stg}	Storage temperature			-65 to 150	°C

5.2 Recommended Operating Conditions

Table 1.26.2. Recommended Operating Conditions (Note 1)

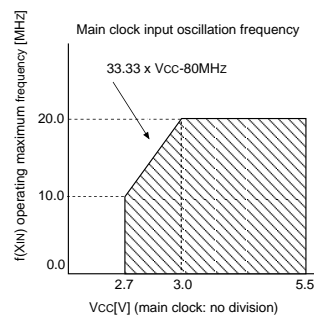
Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage		2.7		5.5	V
AV _{CC}	Analog supply voltage			V _{CC}		V
V _{SS}	Supply voltage			0		V
AV _{SS}	Analog supply voltage			0		V
V _{IH}	HIGH input voltage	RESET, CNV _{SS} , X _{IN} , P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	0.8V _{CC}		V _{CC}	V
		P70, P71	0.8V _{CC}		6.5	V
V _{IL}	LOW input voltage	RESET, CNV _{SS} , X _{IN} , P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	0		0.2V _{CC}	V
I _{OH} (peak)	HIGH peak output current	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107			-10.0	mA
I _{OH} (avg)	HIGH average output current	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107			-5.0	mA
I _{OL} (peak)	LOW peak output current	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107			10.0	mA
I _{OL} (avg)	LOW average output current	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107			5.0	mA
f (X _{IN})	Main clock input oscillation frequency (Note 4)	V _{CC} =3.0 to 5.5V	0		20	MHz
		V _{CC} =2.7 to 3.0V	0		33.33 X V _{CC} -80	MHz
f (X _{CIN})	Sub-clock oscillation frequency			32.768	50	kHz
f (Ring)	On-chip oscillation frequency			1		MHz
f (BCLK)	CPU operation clock		0		20	MHz

Note 1: Referenced to V_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.

Note 2: The mean output current is the mean value within 100ms.

Note 3: The total I_{OL} (peak) for all ports must be 80mA max. The total I_{OL} (peak) for all ports must be -80mA max.

Note 4: Relationship between main clock oscillation frequency and supply voltage.



5.3 A/D Conversion Characteristics

Table 16.3. A/D Conversion Characteristics (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		VREF =VCC				10	Bits
INL	Integral non-linearity error	10 bit	VREF=VCC=5V	AN0 to AN7 input			±3	LSB
			VREF=VCC=3.3V	AN0 to AN7 input			±5	LSB
		8 bit	VREF =VCC=3.3V					±2
–	Absolute accuracy	10 bit	VREF=VCC=5V	AN0 to AN7 input			±3	LSB
			VREF=VCC=3.3V	AN0 to AN7 input			±5	LSB
		8 bit	VREF =VCC=3.3V					±2
DNL	Differential non-linearity error						±1	LSB
–	Offset error						±3	LSB
–	Gain error						±3	LSB
RLADDER	Ladder resistance		VREF =VCC		10		40	kΩ
tCONV	Conversion time(10bit), Sample & hold function available		VREF =VCC=5V, φAD=10MHz		3.3			μs
tCONV	Conversion time(8bit), Sample & hold function available		VREF =VCC=5V, φAD=10MHz		2.8			μs
tsAMP	Sampling time				0.3			μs
VREF	Reference voltage				2.0		VCC	V
VIA	Analog input voltage				0		VREF	V

Note 1: Referenced to VCC=AVCC=VREF=3.3 to 5.5V, VSS=AVSS=0V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.

Note 2: AD operation clock frequency (φAD frequency) must be 10 MHz or less. And divide the fAD if VCC is less than 4.2V, and make φAD frequency equal to or lower than fAD/2.

Note 3: A case without sample & hold function turn φAD frequency into 250 kHz or more in addition to a limit of Note 2.
A case with sample & hold function turn φAD frequency into 1MHz or more in addition to a limit of Note 2.

5.4 Flash Memory Version Electrical Characteristics

Table 16.4. Flash Memory Version Electrical Characteristics (Note 1) 100E/W cycle products (D3, D5, U3, U5)

Symbol	Parameter	Standard			Unit
		Min.	Typ. (Note 2)	Max	
–	Erase/Write cycle (Note 3)	100(Note 4)			cycle
–	Word program time (V _{CC} =5.0V, T _{opr} =25°C)		75	600	μs
–	Block erase time	2Kbyte block	0.2	9	s
		8Kbyte block	0.4	9	s
		16Kbyte block	0.7	9	s
		32Kbyte block	1.2	9	s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend			8	ms
–	Data retention time (Note 5)	20			year

**Table 16.5. Flash Memory Version Electrical Characteristics (Note 6) 10000 E/W cycle products (D7, D9, U7, U9)
[blockA and block B(Note 7)]**

Symbol	Parameter	Standard			Unit
		Min.	Typ. (Note 2)	Max	
–	Erase/Write cycle (Note 3, 8, 9)	10000(Note 4,10)			cycle
–	Word program time (V _{CC} =5.0V, T _{opr} =25°C)		100		μs
–	Block erase time(V _{CC} =5.0V, T _{opr} =25°C) (2Kbyte block)		0.3		s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend			8	ms

Note 1: When not otherwise specified, V_{CC} = 2.7 to 5.5V; T_{opr} = 0 to 60 °C.

Note 2: V_{CC} = 5V; T_{OPR} = 25 °C.

Note 3: Definition of E/W cycle: Each block may be written to a variable number of times - up to a maximum of the total number of distinct word addresses - for every block erase. Performing multiple writes to the same address before an erase operation is prohibited.

Note 4: Maximum number of E/W cycles for which operation is guaranteed.

Note 5: T_{opr} = 55°C.

Note 6: When not otherwise specified, V_{CC} = 2.7 to 5.5V; T_{opr} = -40 to 85°C (D7, U7) / -20 to 85°C (D9, U9).

Note 7: Table 18.5 applies for Block A or B E/W cycles > 1000. Otherwise, use Table 18.4.

Note 8: To reduce the number of E/W cycles, a block erase should ideally be performed after writing as many different word addresses (only one time each) as possible. It is important to track the total number of block erases.

Note 9: Should erase error occur during block erase, attempt to execute clear status register command, then clock erase command at least three times until erase error disappears.

Note 10: When Block A or B E/W cycles exceed 100 (D7, D9, U7, U9), select one wait state per block access. When FMR17 is set to "1", one wait state is inserted per access to Block A or B - regardless of the value of PM17. Wait state insertion during access to all other blocks, as well as to internal RAM, is controlled by PM17 - regardless of the setting of FMR17.

Note 11: Customers desiring E/W failure rate information should contact their Renesas technical support representative.

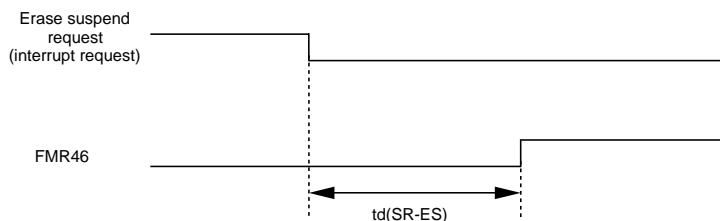


Table 16.6. Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics

Flash program, erase voltage	Flash read operation voltage
V _{CC} = 2.7 V to 5.5 V	V _{CC} =2.7 to 5.5 V

(at T_{opr} = 0 to 60°C)

5.5 Low Voltage Detection Circuit Electrical Characteristics

Table 16.7. Low Voltage Detection Circuit Electrical Characteristics (Note 1, Note 4)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Voltage down detection voltage (Note 1)	V _{CC1} =0.8 to 5.5V	3.3	3.8	4.4	V
Vdet3	Reset level detection voltage (Notes 1, 2)		2.2	2.8	3.6	V
Vdet3s	Low voltage reset retention voltage		0.8			V
Vdet3r	Low voltage reset release voltage (Note 3)		2.2	2.9	4.0	V

Note 1: Vdet4 > Vdet3

Note 2: Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the operation at f(BCLK) ≤ 10MHz is guaranteed.

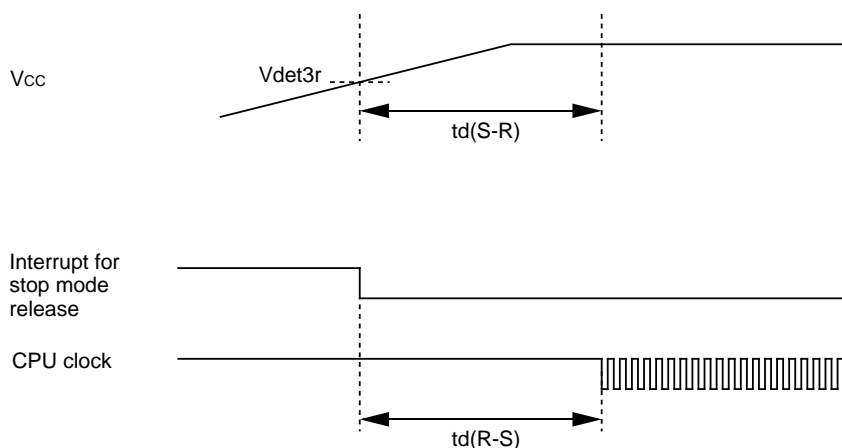
Note 3: Vdet3r > Vdet3 is not guaranteed.

Note 4: The low voltage detection circuit is designed to use when Vcc is set to 5V.

Table 16.8. Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on	V _{CC1} =2.7 to 5.5V			2	ms
td(R-S)	STOP release time				150	μs
td(W-S)	Low power dissipation mode wait mode release time				150	μs
td(M-L)	Time for internal power supply stabilization when main clock oscillation starts				50	μs
td(S-R)	Hardware reset 2 release wait time	V _{CC1} =Vdet3r to 5.5V		6 (Note)	20	ms
td(E-A)	Low voltage detection circuit operation start time	V _{CC1} =2.7 to 5.5V			20	μs

Note : When VCC = 5V



5.6 Electrical Characteristics (V_{CC}=5V)V_{CC} = 5V

Table 16.9. Electrical Characteristics (Note 1)

Symbol	Parameter		Measuring condition	Standard			Unit	
				Min.	Typ.	Max.		
V _{OH}	HIGH output voltage	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	I _{OH} =-5mA	V _{CC} -2.0		V _{CC}	V	
V _{OH}	HIGH output voltage	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	I _{OH} =-200μA	V _{CC} -0.3		V _{CC}	V	
V _{OH}	HIGH output voltage	X _{OUT}	HIGHPOWER			V _{CC} -2.0	V	
			LOWPOWER	I _{OH} =-1mA			V _{CC}	
	HIGH output voltage	X _{COUT}	HIGHPOWER	With no load applied		2.5		V
			LOWPOWER	With no load applied		1.6		
V _{OL}	LOW output voltage	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	I _{OL} =5mA			2.0	V	
V _{OL}	LOW output voltage	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	I _{OL} =200μA			0.45	V	
V _{OL}	LOW output voltage	X _{OUT}	HIGHPOWER	I _{OL} =1mA			2.0	V
			LOWPOWER	I _{OL} =0.5mA			2.0	
	LOW output voltage	X _{COUT}	HIGHPOWER	With no load applied		0		V
			LOWPOWER	With no load applied		0		
V _{T+} -V _{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, INT0 to INT1, INT3 to INT5, NMI, ADTRG, SCL, SDA, RxD0 to RxD2, CTS0 to CTS2, CLK0 to CLK2, TA2OUT to TA4OUT, KI0 to KI3		0.2		1.0	V	
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		2.5	V	
I _{IH}	HIGH input current	P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, X _{IN} , RESET, CNV _{SS}	V _I =5V			5.0	μA	
I _{IL}	LOW input current	P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, X _{IN} , RESET, CNV _{SS}	V _I =0V			-5.0	μA	
R _{PULLUP}	Pull-up resistance	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	V _I =0V	30	50	170	kΩ	
R _{I_XIN}	Feedback resistance	X _{IN}			1.5		MΩ	
R _{I_XCIN}	Feedback resistance	X _{CIN}			15		MΩ	
V _{RAM}	RAM retention voltage		At stop mode	2.0			V	

Note 1: Referenced to V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

VCC = 5V

Table 16.10. Electrical Characteristics (2) (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} =3.0 to 5.5V)	In single-chip mode, the output pins are open and other pins are V _{SS}	Mask ROM	f(BCLK)=20MHz, No division		16	19	mA
				No division, On-chip oscillation		T.B.D		mA
			Flash memory Program	f(BCLK)=10MHz, V _{CC} =5.0V		T.B.D		mA
			Flash memory Erase	f(BCLK)=10MHz, V _{CC} =5.0V		T.B.D		mA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM(Note 3)		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash memory(Note 3)		420		μA
				On-chip oscillation, Wait mode		T.B.D		μA
			Flash memory	f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity High		7.5		μA
				f(BCLK)=32kHz, Wait mode(Note 2), Oscillation capacity Low		2.0		μA
				Stop mode, T _{opr} =25°C		0.8	3.0	μA

Note 1: Referenced to V_{CC}=4.2 to 5.5V, V_{SS}=0V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

Note 2: With one timer operated using fc32.

Note 3: This indicates the memory in which the program to be executed exists.

5.7 Timing Requirements (VCC=5V)**VCC = 5V****(VCC = 5V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)****Table 16.11. External Clock Input (XIN input)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c	External clock input cycle time	50		ns
t _{w(H)}	External clock input HIGH pulse width	25		ns
t _{w(L)}	External clock input LOW pulse width	25		ns
t _r	External clock rise time		15	ns
t _f	External clock fall time		15	ns

VCC = 5V

Timing Requirements

(VCC = 5V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 16.12. Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIn input cycle time	100		ns
t _w (TAH)	TAiIn input HIGH pulse width	40		ns
t _w (TAL)	TAiIn input LOW pulse width	40		ns

Table 16.13. Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIn input cycle time	400		ns
t _w (TAH)	TAiIn input HIGH pulse width	200		ns
t _w (TAL)	TAiIn input LOW pulse width	200		ns

Table 16.14. Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIn input cycle time	200		ns
t _w (TAH)	TAiIn input HIGH pulse width	100		ns
t _w (TAL)	TAiIn input LOW pulse width	100		ns

Table 16.15. Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (TAH)	TAiIn input HIGH pulse width	100		ns
t _w (TAL)	TAiIn input LOW pulse width	100		ns

Table 16.16. Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (UP)	TAiOUT input cycle time	2000		ns
t _w (UPH)	TAiOUT input HIGH pulse width	1000		ns
t _w (UPL)	TAiOUT input LOW pulse width	1000		ns
t _{su} (UP-TiN)	TAiOUT input setup time	400		ns
t _h (TiN-UP)	TAiOUT input hold time	400		ns

Table 16.17. Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIn input cycle time	800		ns
t _{su} (TAiN-TAOUT)	TAiOUT input setup time	200		ns
t _{su} (TAOUT-TAiN)	TAiIn input setup time	200		ns

VCC = 5V

Timing Requirements

(VCC = 5V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 16.18. Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time (counted on one edge)	100		ns
t _w (TBH)	TBiIN input HIGH pulse width (counted on one edge)	40		ns
t _w (TBL)	TBiIN input LOW pulse width (counted on one edge)	40		ns
t _c (TB)	TBiIN input cycle time (counted on both edges)	200		ns
t _w (TBH)	TBiIN input HIGH pulse width (counted on both edges)	80		ns
t _w (TBL)	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 16.19. Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time	400		ns
t _w (TBH)	TBiIN input HIGH pulse width	200		ns
t _w (TBL)	TBiIN input LOW pulse width	200		ns

Table 16.20. Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time	400		ns
t _w (TBH)	TBiIN input HIGH pulse width	200		ns
t _w (TBL)	TBiIN input LOW pulse width	200		ns

Table 16.21. A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (AD)	ADTRG input cycle time (trigger able minimum)	1000		ns
t _w (ADL)	ADTRG input LOW pulse width	125		ns

Table 16.22. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (CK)	CLKi input cycle time	200		ns
t _w (CKH)	CLKi input HIGH pulse width	100		ns
t _w (CKL)	CLKi input LOW pulse width	100		ns
t _d (C-Q)	TxDi output delay time		80	ns
t _h (C-Q)	TxDi hold time	0		ns
t _{su} (D-C)	RxDi input setup time	30		ns
t _h (C-D)	RxDi input hold time	90		ns

Table 16.23. External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (INH)	INTi input HIGH pulse width	250		ns
t _w (INL)	INTi input LOW pulse width	250		ns

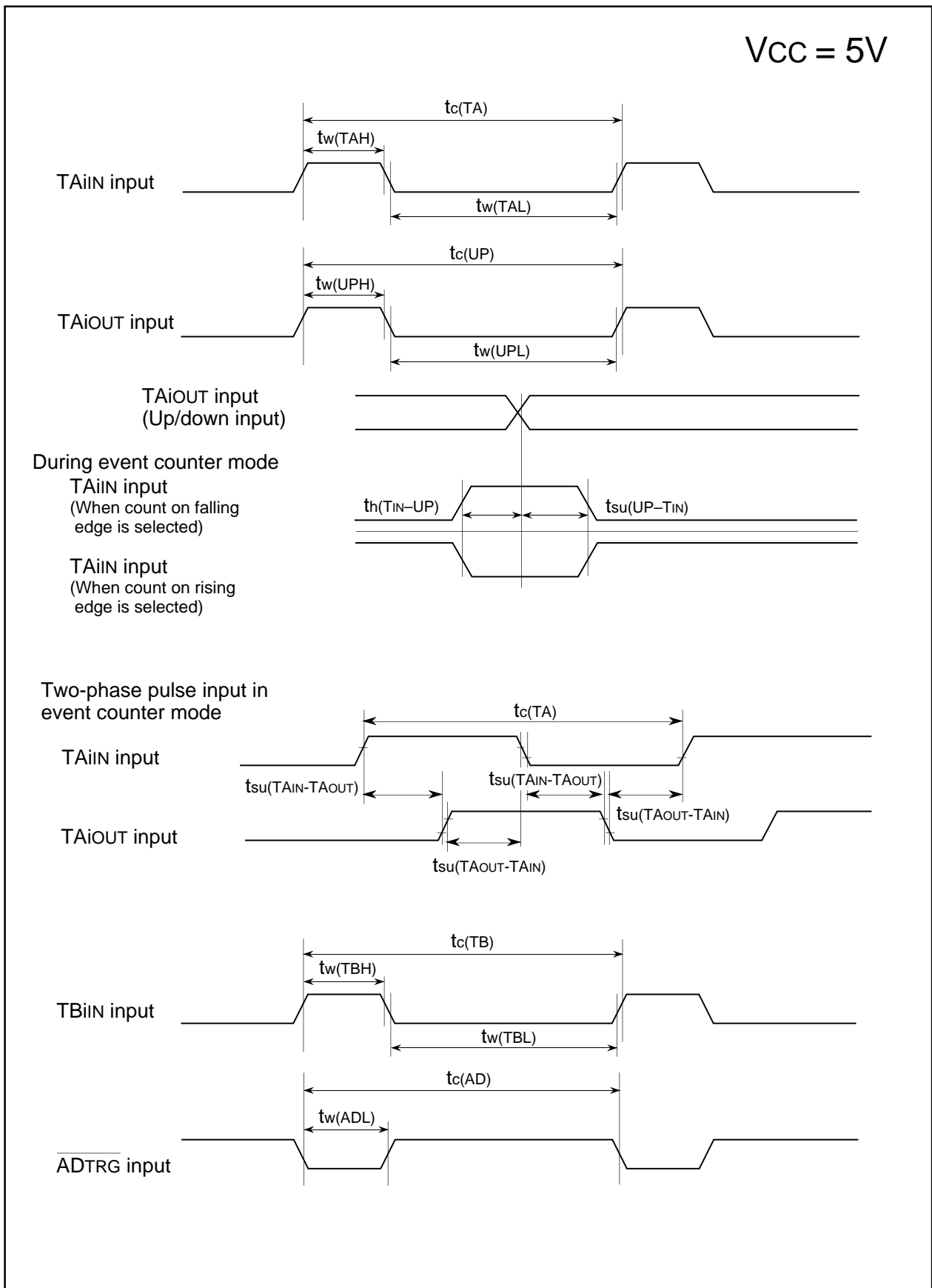


Figure 16.1. Timing Diagram (1)

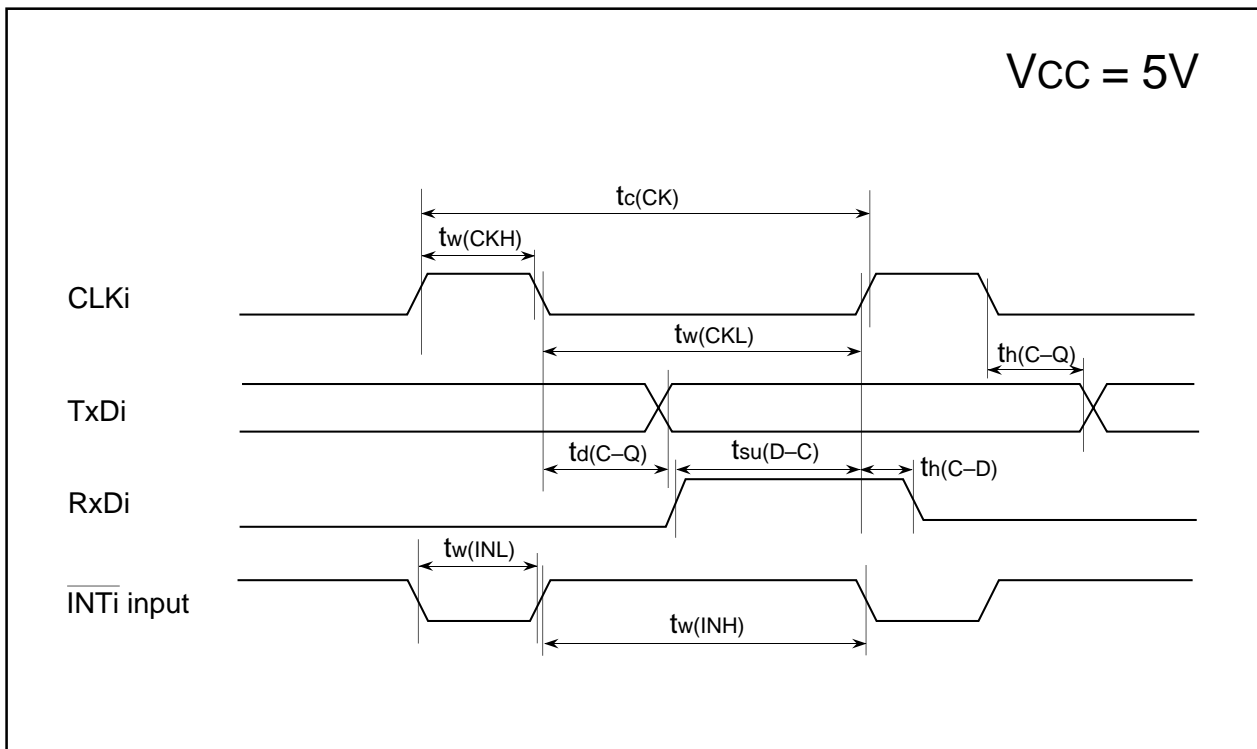


Figure 16.2. Timing Diagram (2)

VCC = 3V

5.8 Electrical Characteristics (VCC=3V)

Table 16.24. Electrical Characteristics (Note)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH output voltage	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	I _{OH} =-1mA	V _{CC} -0.5		V _{CC}	V
V _{OH}	HIGH output voltage	X _{OUT}	HIGHPOWER	I _{OH} =-0.1mA	V _{CC} -0.5	V _{CC}	V
			LOWPOWER	I _{OH} =-50μA	V _{CC} -0.5	V _{CC}	
	HIGH output voltage	X _{COUT}	HIGHPOWER	With no load applied		2.5	V
			LOWPOWER	With no load applied		1.6	
V _{OL}	LOW output voltage	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	I _{OL} =1mA			0.5	V
V _{OL}	LOW output voltage	X _{OUT}	HIGHPOWER	I _{OL} =0.1mA		0.5	V
			LOWPOWER	I _{OL} =50μA		0.5	
	LOW output voltage	X _{COUT}	HIGHPOWER	With no load applied		0	V
			LOWPOWER	With no load applied		0	
V _{T+} -V _{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, INT0 to INT1, INT3 to INT5, NMI, ADTRG, SCL, SDA, RxDo to RxDz, CTS0 to CTS2, CLK0 to CLK2, TA2OUT to TA4OUT, KI0 to KI3		0.2		0.8	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		1.8	V
I _{IH}	HIGH input current	P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, X _{IN} , RESET, CNV _{SS}	V _I =3V			4.0	μA
I _{IL}	LOW input current	P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, X _{IN} , RESET, CNV _{SS}	V _I =0V			-4.0	μA
R _{PULLUP}	Pull-up resistance	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	V _I =0V	50	100	500	kΩ
R _{XIN}	Feedback resistance	X _{IN}			3.0		MΩ
R _{X_CIN}	Feedback resistance	X _{CIN}			25		MΩ
V _{RAM}	RAM retention voltage		At stop mode	2.0			V

Note 1 : Referenced to V_{CC}=2.7 to 3.3V, V_{SS}=0V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

V_{CC} = 3V**Table 16.25. Electrical Characteristics (2) (Note 1)**

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} =2.7 to 3.6V)	In single-chip mode, the output pins are open and other pins are V _{SS}	Flash memory	f(BCLK)=10MHz, No division		8	13	mA
				No division, On-chip oscillation		T.B.D		mA
			Flash memory Program	f(BCLK)=10MHz, V _{CC1} =3.0V		T.B.D		mA
			Flash memory Erase	f(BCLK)=10MHz, V _{CC1} =3.0V		T.B.D		mA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM(Note 3)		25		μA
				f(BCLK)=32kHz, Low power dissipation mode, Flash memory(Note 3)		420		μA
				On-chip oscillation, Wait mode		T.B.D		μA
			Flash memory	f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity High		6.0		μA
				f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity Low		1.8		μA
				Stop mode, T _{opr} =25°C		0.7	3.0	μA

Note 1: Referenced to V_{CC}=2.7 to 3.3V, V_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

Note 2: With one timer operated using fc32.

Note 3: This indicates the memory in which the program to be executed exists.

V_{CC} = 3V**5.9 Timing Requirements (V_{CC}=3V)****Timing Requirements****(V_{CC} = 3V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)****Table 16.26. External Clock Input (X_{IN} input)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c	External clock input cycle time	100		ns
t _{w(H)}	External clock input HIGH pulse width	40		ns
t _{w(L)}	External clock input LOW pulse width	40		ns
t _r	External clock rise time		18	ns
t _f	External clock fall time		18	ns

V_{CC} = 3V**Timing Requirements**(V_{CC} = 3V, V_{SS} = 0V, at T_{opr} = – 20 to 85°C / – 40 to 85°C unless otherwise specified)**Table 16.27. Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time	150		ns
t _w (TAH)	TAiIN input HIGH pulse width	60		ns
t _w (TAL)	TAiIN input LOW pulse width	60		ns

Table 16.28. Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time	600		ns
t _w (TAH)	TAiIN input HIGH pulse width	300		ns
t _w (TAL)	TAiIN input LOW pulse width	300		ns

Table 16.29. Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time	300		ns
t _w (TAH)	TAiIN input HIGH pulse width	150		ns
t _w (TAL)	TAiIN input LOW pulse width	150		ns

Table 16.30. Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (TAH)	TAiIN input HIGH pulse width	150		ns
t _w (TAL)	TAiIN input LOW pulse width	150		ns

Table 16.31. Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (UP)	TAiOUT input cycle time	3000		ns
t _w (UPH)	TAiOUT input HIGH pulse width	1500		ns
t _w (UPL)	TAiOUT input LOW pulse width	1500		ns
t _{su} (UP-TiN)	TAiOUT input setup time	600		ns
t _h (TiN-UP)	TAiOUT input hold time	600		ns

Table 1.6.32. Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time	2		μs
t _{su} (TAiN-TAOUT)	TAiOUT input setup time	500		ns
t _{su} (TAOUT-TAiN)	TAiIN input setup time	500		ns

V_{CC} = 3V**Timing Requirements****(V_{CC} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)****Table 16.33. Timer B Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time (counted on one edge)	150		ns
t _w (TBH)	TBiIN input HIGH pulse width (counted on one edge)	60		ns
t _w (TBL)	TBiIN input LOW pulse width (counted on one edge)	60		ns
t _c (TB)	TBiIN input cycle time (counted on both edges)	300		ns
t _w (TBH)	TBiIN input HIGH pulse width (counted on both edges)	120		ns
t _w (TBL)	TBiIN input LOW pulse width (counted on both edges)	120		ns

Table 16.34. Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time	600		ns
t _w (TBH)	TBiIN input HIGH pulse width	300		ns
t _w (TBL)	TBiIN input LOW pulse width	300		ns

Table 16.35. Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time	600		ns
t _w (TBH)	TBiIN input HIGH pulse width	300		ns
t _w (TBL)	TBiIN input LOW pulse width	300		ns

Table 16.36. A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (AD)	ADTRG input cycle time (trigger able minimum)	1500		ns
t _w (ADL)	ADTRG input LOW pulse width	200		ns

Table 16.37. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (CK)	CLKi input cycle time	300		ns
t _w (CKH)	CLKi input HIGH pulse width	150		ns
t _w (CKL)	CLKi input LOW pulse width	150		ns
t _d (C-Q)	TxDi output delay time		160	ns
t _h (C-Q)	TxDi hold time	0		ns
t _{su} (D-C)	RxDi input setup time	50		ns
t _h (C-D)	RxDi input hold time	90		ns

Table 16.38. External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (INH)	INTi input HIGH pulse width	380		ns
t _w (INL)	INTi input LOW pulse width	380		ns

VCC = 3V

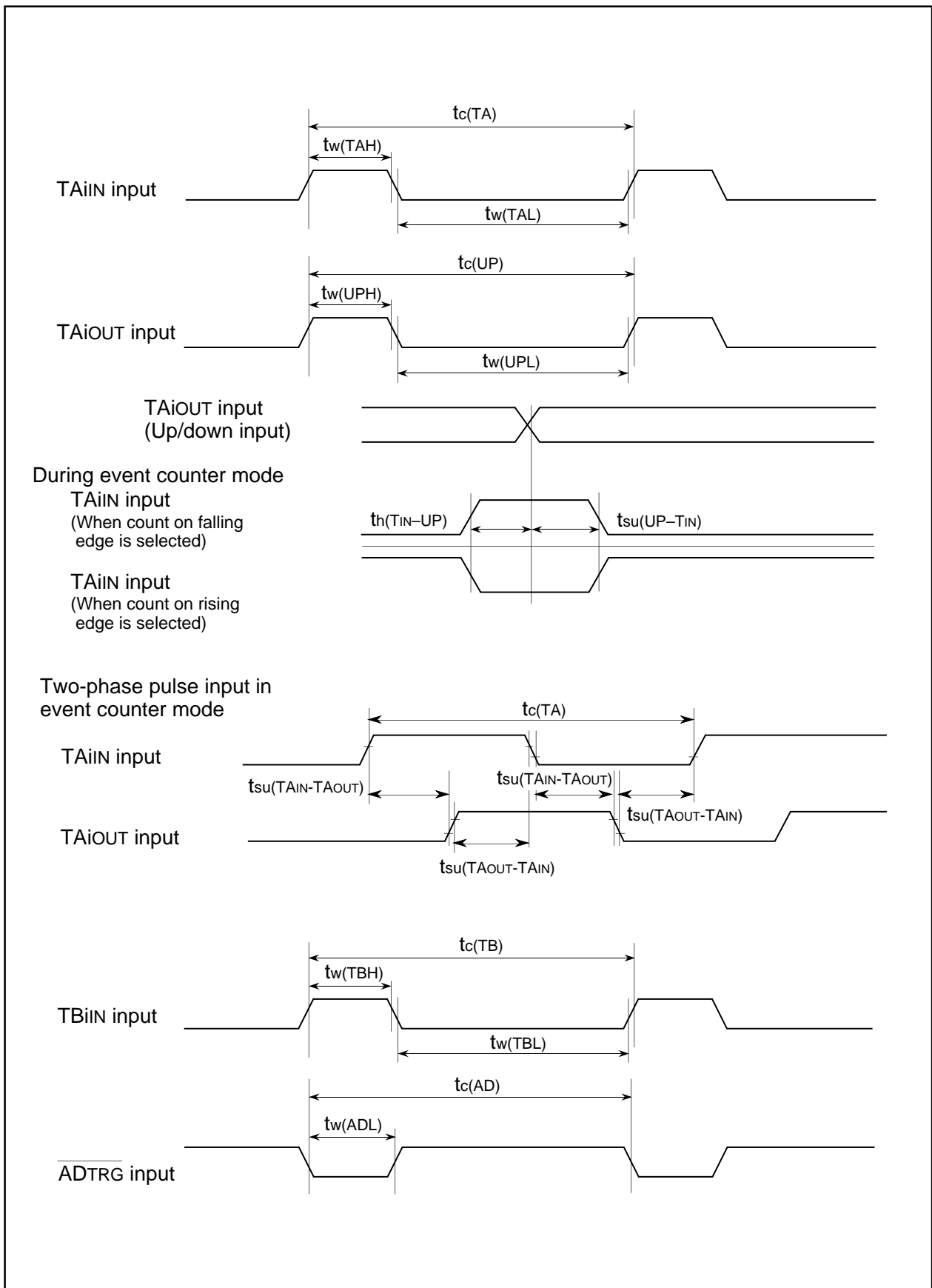


Figure 16.3. Timing Diagram (1)

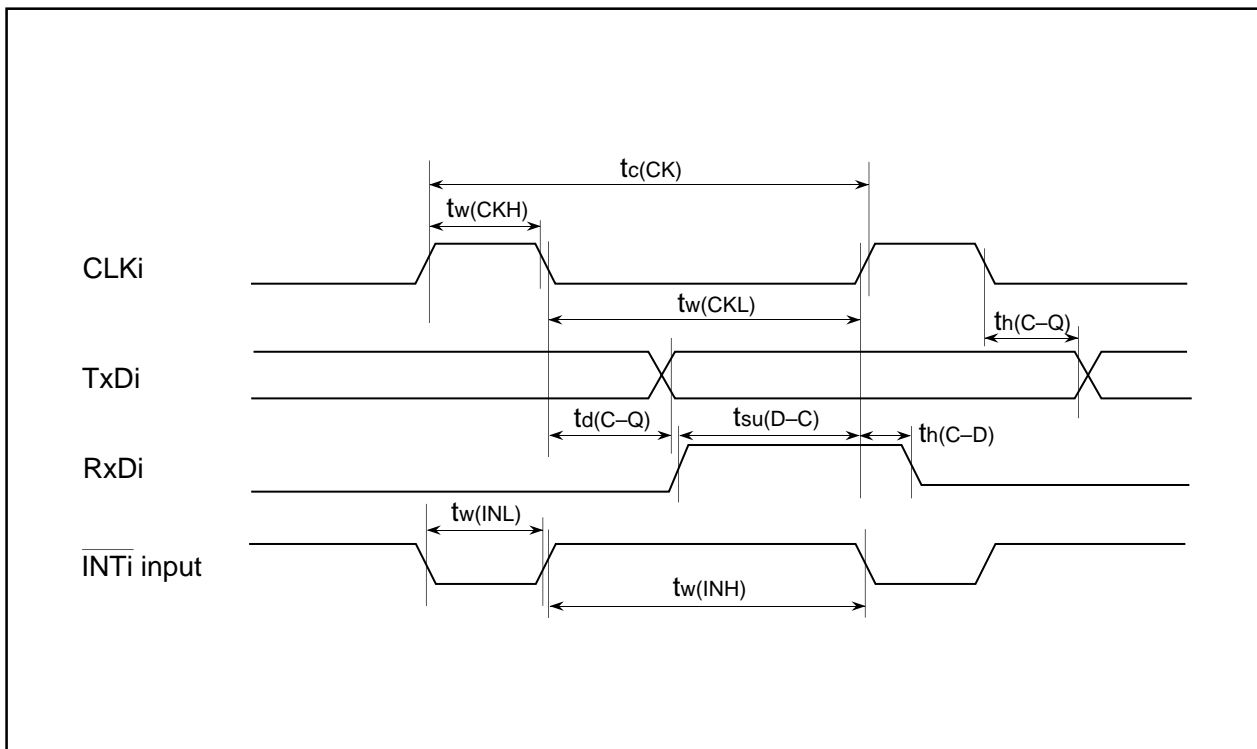
V_{CC} = 3V

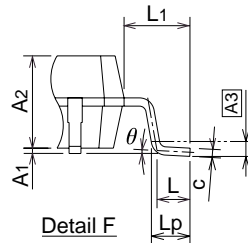
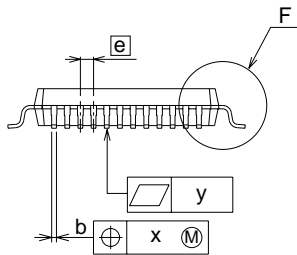
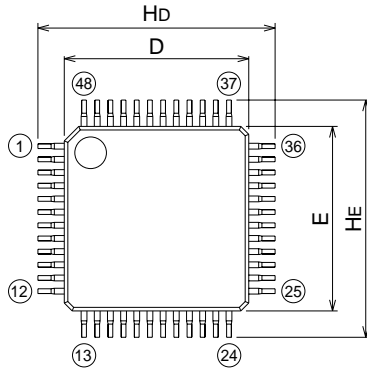
Figure 16.4. Timing Diagram (2)

6. Package

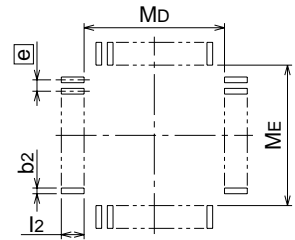
48P6Q-A Recommended

Plastic 48pin 7X7mm body LQFP

EIAJ Package Code LQFP48-P-77-0.50	JEDEC Code -	Weight(g) -	Lead Material Cu Alloy
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Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	-	0.5	-
Hd	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.35	0.5	0.65
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
θ	0°	-	8°
b2	-	0.225	-
l2	1.0	-	-
Md	-	7.4	-
ME	-	7.4	-

REVISION HISTORY

M16C/26 Hardware Manual

Rev.	Date	Description	
		Page	Summary
1.00	Jun/10/ 04	-	First edition

Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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